WHAT IS CLAIMED IS:

1. A method for VLSI chip design comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal paths including resistance and capacitance values.

2. A method according to claim 1 further comprising the step of:

foliating nodes in estimated signal routes.

3. A method according to claim 1 further comprising the step of:

generating a connectivity net list from said model.

4. A method according to claim 1 wherein said step of estimating is performed based on input of a floor plan and a connectivity description.

5. A method according to claim 4 wherein said step of estimating is performed in response to one or more control factor inputs.

6. A method according to claim 5 wherein said control factor input specifies a signal routing algorithm.

7. A method according to claim 4 wherein said step of estimating is performed based on input of signal path configuration parameters.

8. A method according to claim 7 wherein said signal path configuration parameters specify one or more of signal path material, physical size of signal path material or spacing.

9. A method according to claim 7 wherein said step of estimating is performed in response to one or more control factor inputs.

10. A method according to claim 9 wherein said control factor input specifies a signal routing algorithm.

11. A VLSI chip whose design was performed according to a method comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal paths including resistance and capacitance values.

12. A VLSI chip according to claim 11 whose design was performed according to the method further comprising the step of:

foliating nodes in estimated signal routes.

13. A VLSI chip according to claim 11 whose design was performed according to the method further comprising the step of:

generating a connectivity net list from said model.

14. A VLSI chip according to claim 11 whose design was performed according to the method wherein said step of estimating is performed based on input of a floor plan and a connectivity description.

15. A VLSI chip according to claim 14 whose design was performed according to the method wherein said step of estimating is performed in response to one or more control factor inputs.

16. A VLSI chip according to claim 15 whose design was performed according to the method wherein said control factor input specifies a signal routing algorithm.

17. A VLSI chip according to claim 14 whose design was performed according to the method wherein said step of estimating is performed based on input of signal path configuration parameters.

18. A VLSI chip according to claim 17 whose design was performed according to the method wherein said signal path configuration parameters specify one or more of signal path material, physical size of signal path material or spacing.

19. A VLSI chip according to claim 17 whose design was performed according to the method wherein said step of estimating is performed in response to one or more control factor inputs.

20. A VLSI chip according to claim 19 whose design was performed according to the method wherein said control factor input specifies a signal routing algorithm.